查询SY100EL05ZC供应商

2-INPUT DIFFERENTIAL AND/NAND

FEATURES

- **275ps propagation delay**
- **High bandwidth output transitions**
- **Internal 75KΩ input pull-down resistors**
- **Available in 8-pin SOIC package**

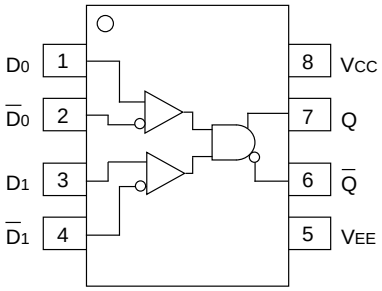
DESCRIPTION

The SY10/100EL05 are 2-input differential AND/NAND gates. These devices are functionally equivalent to the E404 devices, with higher performance capabilities. With propagation delays and output transition times significantly faster than the E404, the EL05 is ideally suited for those applications which require the ultimate in AC performance.

Because a negative 2-input NAND is equivalent to a 2-input OR function with inverted inputs, the differential inputs and outputs of the device allows the EL05 to also be used as a 2-input differential OR/NOR gate.

The differential inputs employ clamp circuitry so that, under open conditions (pulled down to V_{EE}), the input to the AND gate will be HIGH. In this way, if one set of inputs is open, the gate will remain active to the other input.

PIN CONFIGURATION/BLOCK DIAGRAM



SOIC
TOP VIEW

PIN NAMES

Pin	Function
D_0, D_1	Data Inputs
Q	Data Outputs

Rev.: E Amendment: /0
Issue Date: August, 1998

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND

Symbol	Parameter	T_A = –40°C			T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{EE}	Power Supply Current													mA
	10EL	—	18	22	14	18	22	14	18	22	14	18	22	
	100EL	—	18	22	14	18	22	14	18	22	16	21	25	
V_{EE}	Power Supply Voltage													V
	10EL	–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	
	100EL	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	—	—	150	µA

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND

Symbol	Parameter	T_A = –40°C			T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{PLH} t_{PHL}	Propagation Delay to Output D	135	260	440	185	275	390	185	275	390	215	305	420	ps
V_{PP}	Minimum Input Swing[1]	150	—	—	150	—	—	150	—	—	150	—	—	mV
V_{CMR}	Common Mode Range[2]	(2)	—	–0.4	(2)	—	–0.4	(2)	—	–0.4	(2)	—	–0.4	V
t_r t_f	Output Rise/Fall Times Q (20% to 80%)	100	225	350	100	225	350	100	225	350	100	225	350	ps

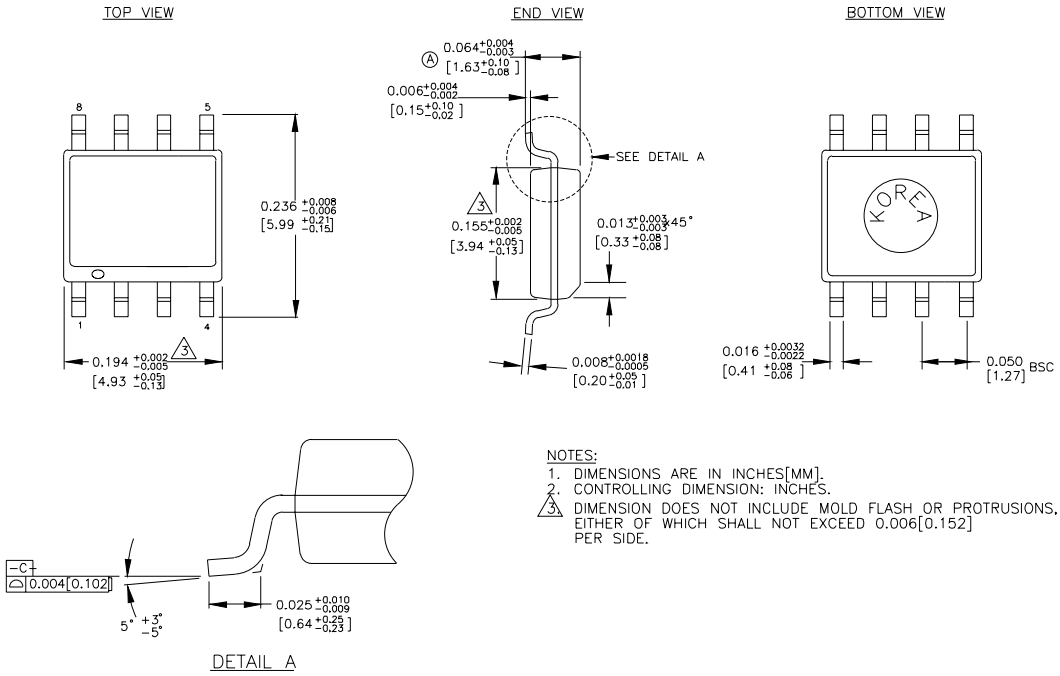
NOTES:

1. Minimum input swing for which AC parameters are guaranteed. The device has a DC gain of ≈40.
2. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP} min. and 1V. The lower end of the CMR range is dependent on V_{EE} and is equal to V_{EE} + 3.0V.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10EL05ZC	Z8-1	Commercial
SY10EL05ZCTR	Z8-1	Commercial
SY100EL05ZC	Z8-1	Commercial
SY100EL05ZCTR	Z8-1	Commercial

8 LEAD SOIC .150" WIDE (Z8-1)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.006[0.152] PER SIDE.

Rev. 03

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